SpiderCat: Optimal Fault-Tolerant Cat State Preparation

Andrey Boris Khesin Sarah Meng Li Boldizsár Poór

Benjamin Rodatz John van de Wetering Richie Yeung

The full technical manuscript of this work can be found at https://arxiv.org/abs/2603.05391.

As larger quantum computing devices become available, the first experimental demonstrations of fault-tolerant quantum computation have begun to emerge [2, 3, 1, 29, 35]. These results show that, by carefully structuring unitaries and measurements, it is possible to suppress the propagation of physical errors, detect faults as they occur, and actively correct them. In contrast to the classical setting where error correction is typically confined to communication and storage, in quantum computing every gate, measurement, and even idle qubit is inherently noisy [6, 12, 16]. As a result, fault tolerance must be treated as a global design constraint: the entire circuit architecture must be engineered so that errors remain controlled throughout the computation [15, 18, 26, 31].

While the foundational feasibility results for fault-tolerant quantum computing have been established for decades [4, 17, 32], it is only in recent years that fault-tolerant compilation has emerged as an active area of research, with protocols that aggressively optimise individual components of fault-tolerant circuits [27, 28, 10, 8, 7, 9, 13]. A particular component that has received a lot of attention is the fault-tolerant preparation of stabiliser states for specific (small) codes. Existing approaches include reinforcement learning [34, 25], constraint-satisfaction solvers [22], brute-force search [13], and systematic analyses of error propagation and verification circuits [21, 14, 19], all aimed at constructing fault-tolerant state-preparation circuits for specific, typically small, codes.

Although these methods are effective for circuits of up to roughly 30–70 qubits (depending on the approach) and under the assumption of low-weight errors, they do not readily scale, as they rely on analysing all possible errors across the entire circuit, either directly or through carefully tailored problem reductions. Here, we present a fundamentally different approach to stabiliser-state preparation, with a focus on the fault-tolerant preparation of *CAT states* (i.e. generalised GHZ states) of the form $(|0\cdots0\rangle+|1\cdots1\rangle)/\sqrt{2}$. These states are a key primitive for constructing general stabiliser states [13], implementing Shor-style syndrome extraction [32, 33, 11] (including optimised variants [28]), realising fault-tolerant logical operations [30, 5], enabling magic-state distillation [9, 14], and serving as an important benchmark for quantum hardware [36].

In [20], we present SpiderCat, a scalable construction for provably optimal t-fault-tolerant CAT-state preparation across wide parameter regimes (i.e., large CAT states with improved fault tolerance). Building on [28, 27], we represent circuits as ZX-diagrams and optimise them via fault-equivalent rewrites, so their behaviour under noise is preserved. This perspective reduces fault-tolerant CAT-state preparation to a graph-theoretic construction problem, as we outline below.

First, as a simple demonstration of the utility of this approach we find an intuitive construction of t-fault-tolerant n-qubit *CAT states* which have an improved circuit depth of $O(\log t)$ compared to the previous $O(\log n)$ of [23], while not requiring the expensive solving of large SAT instances which restrict that method to $n \leq 70$ and $t \leq 3$ (or $n \leq 30$ for $t \leq 7$).

Theorem 1. *We can efficiently construct n-qubit t-FT CAT states using $n(1+\log(t+1))-2(t+1)$ CNOT gates, $n/2$ ancillas and in CNOT depth $2\log t + 2$.*

Method	**CNOT count**	**Depth**	**Ancillas**	**max t**	**max n**
FA [13]	$O(n)$	$O(n)$	$O(n)$	6	24
PWW [23]	$\leq 3n$	$O(\log n)$	n	9	19
CB [7]	$O(n)$	$O(n)$	$O(n)$	5	8
Recursive	$n\log(t+1)+n$	$2\log(t+1)+2$	$\leq \frac{1}{2}\boldsymbol{n}$	$\boldsymbol{\infty}$	$\boldsymbol{\infty}$
Optimal (deep || SAT)	$\boldsymbol{(r_t+1)n+1}$	$\leq (r_t+1)n+1$	$\leq \frac{r_t}{2}\boldsymbol{n+1}$	$5 \,\|\|\, 7$	$\boldsymbol{\infty} \,\|\|\, 50$
Optimal (shallow)	$\leq \left(\frac{29r_t+26}{10}\right) n$	$\mathbf{3}$	$\left(\frac{12r_t+8}{5}\right) n$	5	$\boldsymbol{\infty}$
Ramanujan (some n)	$\leq 37.4n$	$\mathbf{3}$	$\leq 30.4n$	$\boldsymbol{\infty}$	$\boldsymbol{\infty}$
Ramanujan (all n)	$\leq 5\times 10^6 n$	$\mathbf{3}$	$\leq 4\times 10^6 n$	$\boldsymbol{\infty}$	$\boldsymbol{\infty}$

Table 1: Comparison of different n-qubit CAT-state preparation methods that are fault-tolerant up to faults of weight t. Depth is the CNOT depth, and Ancillas is the maximum number of ancilla in use at one time, with reuse allowed. The number r_t is the optimal *vertex ratio* of Theorem 3. The max value of n is reported for the largest t. In the row labelled 'Optimal (deep || SAT)", we report results obtained from the graph-theoretic constructions and circuits found using constraint satisfaction.

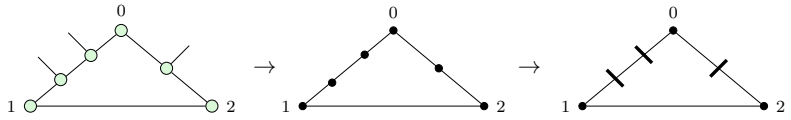

Figure 1: An example of a Z-graph, its underlying graph, and its underlying marked graph.

We then study how we can find circuits preparing t-FT CAT states with an optimal number of CNOT gates. We generalise the idea behind the construction above by considering general phase-free ZX-diagrams consisting solely of Z-spiders of arity 3, which we treat as a type of 3-regular graph we call a *Z-graph*; see Figure 1. From such a graph with k vertices we can construct a circuit that prepares a CAT state with $k+1$ CNOTs, which is shown in detail in Figure 2. This is the most general construction we need to consider due to the following result.

Theorem 2. *Let C be a circuit consisting of CNOTs, ancilla preparations and post-selected measurements containing k CNOT gates, which t-fault-tolerantly prepares the n-qubit CAT state. Then we can efficiently find an underlying Z-graph containing at most $k-1$ spiders, which also t-fault-tolerantly prepares the n-qubit CAT state using at most k CNOT gates.*

Then we show that a Z-graph that t-fault-tolerantly prepares a CAT state is 'resistant' to being disconnected by a set of edge cuts on at most t edges, a property we call being *t-robust*. This allows us to use techniques from graph theory to derive for the first time concrete lower bounds on the number of CNOT gates required to implement a fault-tolerant CAT state. In particular, we consider *marked* 3-regular graphs, where certain edges are allowed to have a mark denoting that we could have an output wire there (see Figure 1). A graph with k vertices and n marks would then correspond to an n-qubit CAT state with $k+1$ CNOT gates. This allows us to define a *vertex ratio* $r = k/n$ which we then want to optimise over the set of graphs that t-FT prepare a CAT state.

Theorem 3. *Let r_t^n be the minimum vertex ratio over all t-*robust *graphs with n marks and let $r_t := \inf_n r_t^n$ be the optimal ratio for a given t. Then we have the following values for $t \leq 5$: $r_1 = 0$, $r_2 = \frac{1}{3}$, $r_3 = \frac{2}{3}$, $r_4 = \frac{5}{6}$ and $r_5 = 1$. Furthermore we have $r_\infty := \liminf_n \sup_t r_t^n \leq 12$. Moreover, for each of these cases there exists an infinite family of graphs that achieves these optimal ratios.*

Proposition 1. *Any CNOT circuit that t-fault-tolerantly prepares the n-qubit CAT state contains at least $n(r_t+1)+1$ CNOT gates.*

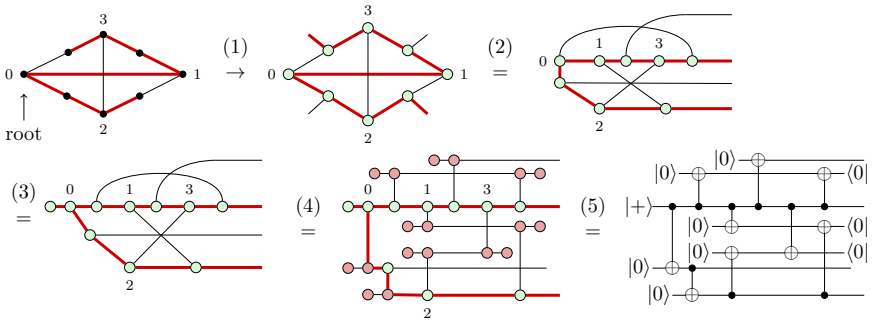

Figure 2: A demonstration of how we go from a marked 3-regular graph to a circuit for a CAT state. The red line denotes a chosen spanning tree, which in this case is a path. Each mark on an edge corresponds to a Z-spider with an output wire after (1). In (2) we lay out the spiders using the spanning tree. Then we use some fault-equivalent rewrites to turn this into a CNOT circuit involving ancilla preparations and post-selections, which can be viewed as added flags in the circuit.

The inequality $r_\infty \leq 12$ is achieved by constructing suitable *Ramanujan graphs* that are t-robust for arbitrary t. We can find a family of such Ramanujan graphs of increasing size V_k which have at most a constant size ratio $V_k/V_{k-1} = O(1)$ between them, which also gives us a way to construct CAT states up to arbitrary levels of fault-tolerance by 'rounding up' to the nearest graph in this family.

Corollary 1. *There exists a constant C such that any n-qubit CAT state can be constructed fault-equivalently using at most $C \cdot n$ three-legged spiders. In particular, we can construct t-FT n-qubit CAT states with t arbitrarily high using $O(n)$ CNOT gates.*

Combining Theorem 2, Proposition 1 and Theorem 3, we see that if we can find a t-robust graph with the exact optimal vertex ratio for a given number of n marks, that this would result in a circuit preparing a t-FT n-qubit CAT state with an optimal number of CNOT gates. We show how such graphs can be generated in practice. We do this by restricting the search to 3-regular cycle graphs which have a Hamiltonian path by construction. We then stochastically update the connectivity to optimise certain graph metrics that relate to t-robustness. Once we have a t-robust graph, we use a constraint satisfaction solver to find the maximum number of marks we can put on this graph.

Simulation and Benchmarking All scripts, circuits, benchmarking/visualisation code, and simulation data are available in [24]. By encoding optimal graph construction as a constraint satisfaction problem, we find explicit constructions for circuits meeting the CNOT lower bound for all $n \leq 50$ and $t \leq 5$, and for nearly all (n, t) pairs with $n \leq 100$ and $t \leq 5$ or $n \leq 50$ and $t \leq 7$, substantially extending the achievable (n, t) regime while further reducing the resource overhead.

Across a broad range of (n, t), benchmarks against Flag-at-Origin [13] and MQT [23] show that SpiderCat achieves the lowest overhead at comparable fault-tolerant performance. It scales to larger CAT sizes and higher target distances by reducing the problem of fault-tolerant CAT-state preparation to a tractable graph-theoretic construction.

Conclusions By representing circuits as ZX-diagrams and optimising via fault-equivalent rewrites, SpiderCat yields circuits that are fault-tolerant by construction with provably optimal CNOT overhead. Since CAT states underpin CSS state preparation and Shor-style syndrome extraction, our results provide a foundation for more scalable, resource-efficient fault-tolerant compilation across a wide range of protocols.

References

[1] Mohamed H Abobeih, Yu Wang, John Randall, SJH Loenen, Christina E Bradley, Matthew Markham, Daniel J Twitchen, Barbara M Terhal, and Tim H Taminiau. Fault-tolerant operation of a logical qubit in a diamond quantum processor. *Nature*, 606(7916):884–889, 2022.

[2] Google Quantum AI. Suppressing quantum errors by scaling a surface code logical qubit. *Nature*, 614(7949):676–681, 2023.

[3] Google Quantum AI and Collaborators. Quantum error correction below the surface code threshold. *Nature*, 638(8052):920–926, 2025.

[4] Panos Aliferis and John Preskill. Fault-tolerant quantum computation against biased noise. *Phys. Rev. A*, 78:052331, Nov 2008.

[5] Friederike Butt, Sascha Heußen, Manuel Rispler, and Markus Müller. Fault-tolerant code-switching protocols for near-term quantum processors. *PRX Quantum*, 5:020345, May 2024.

[6] Zhenyu Cai, Ryan Babbush, Simon C. Benjamin, Suguru Endo, William J. Huggins, Ying Li, Jarrod R. McClean, and Thomas E. O'Brien. Quantum error mitigation. *Rev. Mod. Phys.*, 95:045005, Dec 2023.

[7] Christopher Chamberland and Michael E. Beverland. Flag fault-tolerant error correction with arbitrary distance codes. *Quantum*, 2:53, February 2018.

[8] Christopher Chamberland and Andrew W. Cross. Fault-tolerant magic state preparation with flag qubits. *Quantum*, 3:143, May 2019.

[9] Christopher Chamberland and Kyungjoo Noh. Very low overhead fault-tolerant magic state preparation using redundant ancilla encoding and flag qubits. *npj Quantum Information*, 6(1):91, 2020.

[10] Rui Chao and Ben W Reichardt. Fault-tolerant quantum computation with few qubits. *npj Quantum Information*, 4(1):42, 2018.

[11] Guillermo Escobar-Arrieta and Mauricio Gutiérrez. Improved performance of the bacon-shor code with steane's syndrome extraction method. *Phys. Rev. A*, 111:032427, Mar 2025.

[12] Samuele Ferracin, Akel Hashim, Jean-Loup Ville, Ravi Naik, Arnaud Carignan-Dugas, Hammam Qassim, Alexis Morvan, David I. Santiago, Irfan Siddiqi, and Joel J. Wallman. Efficiently improving the performance of noisy quantum computers. *Quantum*, 8:1410, July 2024.

[13] Diego Forlivesi and David Amaro. Flag at origin: a modular fault-tolerant preparation for css codes. *arXiv preprint arXiv:2508.14200*, 2025.

[14] Hayato Goto. Minimizing resource overheads for fault-tolerant preparation of encoded states of the Steane code. *Scientific Reports*, 6(1):19578, 2016.

[15] Daniel Gottesman. *Stabilizer codes and quantum error correction*. California Institute of Technology, 1997.

[16] Daniel Gottesman. An introduction to quantum error correction and fault-tolerant quantum computation. *arXiv preprint arXiv:0904.2557*, 2009.

[17] Daniel Gottesman. Fault-tolerant quantum computation with constant overhead. *arXiv preprint arXiv:1310.2984*, 2013.

[18] Daniel Gottesman. *Surviving as a Quantum Computer in a Classical World*. Maryland, Maryland, 2024.

[19] Naoyuki Kanomata and Hayato Goto. Fault-tolerant quantum computing with a high-rate symplectic double code. *arXiv preprint arXiv:2509.15457*, 2025.

[20] Andrey Boris Khesin, Sarah Meng Li, Boldizsár Poór, Benjamin Rodatz, John van de Wetering, and Richie Yeung. SpiderCat: Optimal fault-tolerant CAT state preparation. *arXiv preprint arXiv:2603.05391*, 2026.

[21] Adam Paetznick and Ben W. Reichardt. Fault-tolerant ancilla preparation and noise threshold lower bounds for the 23-qubit Golay code. *Quant. Inf. Comput.*, 12(11-12):1034–1080, 2012.

[22] Tom Peham, Ludwig Schmid, Lucas Berent, Markus Müller, and Robert Wille. Automated synthesis of fault-tolerant state preparation circuits for quantum error-correction codes. *PRX Quantum*, 6:020330, May 2025.

[23] Tom Peham, Erik Weilandt, and Robert Wille. Optimizing fault-tolerant cat state preparation. *arXiv preprint arXiv:2601.03343*, 2026.

[24] Boldizsár Poór. Implementation and simulation of SpiderCat: Optimal fault-tolerant CAT state preparation. `https://github.com/boldar99/spidercat`, 2026.

[25] Riccardo Porotti, Antoine Essig, Benjamin Huard, and Florian Marquardt. Deep Reinforcement Learning for Quantum State Preparation with Weak Nonlinear Measurements. *Quantum*, 6:747, June 2022.

[26] John Preskill. Fault-tolerant quantum computation. *Introduction to quantum computation and information*, 213, 1998.

[27] Benjamin Rodatz, Boldizsár Poór, and Aleks Kissinger. Floquetifying stabiliser codes with distance-preserving rewrites. *arXiv preprint arXiv:2410.17240*, 2024.

[28] Benjamin Rodatz, Boldizsár Poór, and Aleks Kissinger. Fault tolerance by construction. *arXiv preprint arXiv:2506.17181*, 2025.

[29] Pedro Sales Rodriguez, John M Robinson, Paul Niklas Jepsen, Zhiyang He, Casey Duckering, Chen Zhao, Kai-Hsin Wu, Joseph Campo, Kevin Bagnall, Minho Kwon, et al. Experimental demonstration of logical magic state distillation. *Nature*, 645(8081):620–625, 2025.

[30] Abhi Kumar Sharma and Shayan Srinivasa Garani. Fault-tolerant quantum ldpc encoders. In *2024 IEEE International Symposium on Information Theory Workshops (ISIT-W)*, pages 1–6, 2024.

[31] Peter W Shor. Fault-tolerant quantum computation. In *Proceedings of 37th conference on foundations of computer science*, pages 56–65. IEEE, 1996.

[32] P.W. Shor. Fault-tolerant quantum computation. In *Proceedings of 37th Conference on Foundations of Computer Science*, pages 56–65, 1996.

[33] Theerapat Tansuwannont, Balint Pato, and Kenneth R. Brown. Adaptive syndrome measurements for Shor-style error correction. *Quantum*, 7:1075, August 2023.

[34] Remmy Zen, Jan Olle, Luis Colmenarez, Matteo Puviani, Markus Müller, and Florian Marquardt. Quantum circuit discovery for fault-tolerant logical state preparation with reinforcement learning. *Phys. Rev. X*, 15:041012, Oct 2025.

[35] Jiaxuan Zhang, Zhao-Yun Chen, Yun-Jie Wang, Bin-Han Lu, Hai-Feng Zhang, Jia-Ning Li, Peng Duan, Yu-Chun Wu, and Guo-Ping Guo. Demonstrating a universal logical gate set in error-detecting surface codes on a superconducting quantum processor. *npj Quantum Information*, 11(1):177, 2025.

[36] Zoltán Zimborás, Attila Portik, David Aguirre, Rubén Peña, Domonkos Svastits, András Pályi, Áron Márton, János K Asbóth, Anton Frisk Kockum, Mikel Sanz, et al. The eu quantum flagship's key performance indicators for quantum computing. *arXiv preprint arXiv:2512.19653*, 2025.